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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,290	01/14/2002	Jong-Hong Bae	123037-05005038	4722

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EXAMINER	
SMITHERS, MATTHEW	
ART UNIT	**PAPER NUMBER**
2137	

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,290	BAE, JONG-HONG	
	Examiner	Art Unit	
	Matthew B. Smithers	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/07/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement filed May 7, 2004 has been placed in the application file and the information referred to therein has been considered as to the merits.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. patent 5,416,783 granted to Broseghini et al.

Regarding claim 1, Broseghini meets the claimed limitations as follows: "An apparatus for protecting data outputted from a code read only memory (ROM), comprising:

a first encryption means for encrypting data outputted from the code ROM;

a second encryption means for generating a read enable signal through an encryption process; and

an output means for dumping out the encrypted data outputted from the first encryption means in response to the read enable signal outputted from the second

encryption means." see column 11, line 62 to column 15, line 56; figure 2 module 26 (ROM) and figure 10.

Regarding claim 2, Broseghini meets the claimed limitations as follows: "The apparatus of claim 1, wherein the first encryption means including:
a multiple input signature analysis register (MISR) for compressing data outputted from the code ROM in synchronization with a clock signal;
and an initializing means for providing an initialization value to the MISR unit in response to a test enable signal and a reset signal." see column 4, lines 39-59; column 11, line 62 to column 15, line 56; figure 2 module 26 (ROM) and figure 10.

Regarding claim 3, Broseghini meets the claimed limitations as follows: "The apparatus of claim 2, wherein the initializing means includes a transistor, which provides the initialization value to the MISR unit when all the test enable signal and the reset signal are enabled." see column 4, lines 39-59; column 11, line 62 to column 15, line 56; figure 2 module 26 (ROM) and figure 10.

Regarding claim 4, Broseghini meets the claimed limitations as follows: "The apparatus of claim 1, wherein the second encryption means including: a control state machine unit for generating a control signal for a ROM test operation in response to the test enable signal and the clock signal; a MISR unit for inputting, inputting and compressing key data in synchronization with the clock signal; an initializing means for providing an initialization value to the MISR unit in response to the test enable signal and the reset signal; and a comparison unit for outputting the read enable signal by comparing a value outputted from the MISR unit with an expected value." see column 6,

lines 7-29; column 7, lines 48-57; column 8, lines 41-50; column 11, line 62 to column 15, line 56; figure 2 and figure 10.

Regarding claim 5, Broseghini meets the claimed limitations as follows: "The apparatus of claim 4, wherein the expected value is a value generated in a condition of recognizing the initialization value and the key data." see column 8, lines 41-50 and column 12, lines 3-10.

Regarding claim 6, Broseghini meets the claimed limitations as follows: "The apparatus of claim 4, wherein the control state machine unit includes an initial state, a finish state and a plurality of internal states, wherein the control state machine unit transits to the initial state in response to a reset signal, wherein the control state machine unit sequentially transits to a plurality of internal states in response to the test enable signal and the clock signal, wherein the control state machine unit in the final internal state, finally transits to the finish state, wherein the control state machine unit outputs the enabled control signal in the initial state and in the plurality of internal states, and wherein the control state machine unit outputs the control signal in the final state." see column 6, lines 7-29; column 7, lines 48-57; column 11, line 62 to column 15, line 56; and figure 10.

Regarding claim 7, Broseghini meets the claimed limitations as follows:

"The apparatus of claim 4, wherein the control state machine unit equips the internal state as much as the number of the key data." see column 12, lines 55-65.

Regarding claim 8, Broseghini meets the claimed limitations as follows: "The apparatus of claim 4, wherein the comparison means outputs the read enable

signal when the compressing value outputted from the MISR unit and the initialization value are the same." see column 8, lines 41-49.

Regarding claim 9, Broseghini meets the claimed limitations as follows: "The apparatus of claim 4, wherein the initializing means includes a transistor, which provides the initialization value to the MISR unit when all the test enable signal and the reset signal are enabled." see column 6, lines 7-29; column 7, lines 48-57; column 11, line 62 to column 15, line 56; and figure 10.

Regarding claim 10, Broseghini meets the claimed limitations as follows: "The apparatus of claim 4, wherein the output means includes a logic multiplication means for ANDing the encrypted data outputted from the first encryption means and the read enable signal." see column 5, lines 14-27.

Regarding claim 11, Broseghini meets the claimed limitations as follows: "An apparatus for protecting data outputted from a code ROM, comprising:
a control state machine unit for generating a control signal for a ROM test operation in response to the test enable signal and the clock signal;
a MISR unit for inputting, compressing key data in synchronization with the clock signal in response to the test enable signal;

an initializing means for providing an initialization value to the MISR unit in response to the test enable signal and the reset signal; a comparison unit for outputting the read enable signal by comparing value outputted from the MISR unit with an expected value; and an output means for dumping the code ROM data in response to a read enable signal." see column 6, lines 7-29; column 7, lines 48-57; column 8, lines 41-

50; column 11, line 62 to column 15, line 56; figure 2 and figure 10.

Regarding claim 12, Broseghini meets the claimed limitations as follows: "The apparatus of claim 11, wherein the initialization value is a value generated in a condition of recognizing the initialization value and the key data." see column 8, lines 41-50 and column 12, lines 3-10.

Regarding claim 13, Broseghini meets the claimed limitations as follows: "The apparatus of claim 11, wherein the control state machine unit includes an initial state, a finish state and lots of internal states, and the control state machine unit transits to the initial state, the lots of internal states, sequentially, and to the finish state, finally, in response to a reset signal, the test enable signal and the clock signal, and in the final internal state, respectively, and then, the initial state and the lots of internal states output the enabled control signal, and the final state outputs disabled the control signal." see column 6, lines 7-29; column 7, lines 48-57; column 11, line 62 to column 15, line 56; and figure 10.

Regarding claim 14, Broseghini meets the claimed limitations as follows: "The apparatus of claim 11, wherein the control state machine unit equips the internal state as much as the number of the key data." see column 12, lines 55-65.

Regarding claim 15, Broseghini meets the claimed limitations as follows: "The apparatus of claim 11, wherein the comparison means outputs enabled the read enable signal when the compressing value outputted from the MISR unit and the initialization value are the same." see column 8, lines 41-49.

Regarding claim 16, Broseghini meets the claimed limitations as follows:

"The apparatus of claim 11, wherein the initializing means includes a transistor, which provides the initialization value to the MISR unit when all the test enable signal and the reset signal are enabled." see column 6, lines 7-29; column 7, lines 48-57; column 11, line 62 to column 15, line 56; and figure 10.

Regarding claim 17, Broseghini meets the claimed limitations as follows: "The apparatus of claim 11, wherein the output means includes a logic multiplication means for ANDing the encrypted data outputted from the first encryption means and the read enable signal." see column 5, lines 14-27.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-17 rejected under 35 U.S.C. 102(e) as being anticipated by U.S. patent 6,321,320 granted to Fleischman et al.

Regarding claim 1, Fleischman meets the claimed limitations as follows: "An apparatus for protecting data outputted from a code read only memory (ROM), comprising:

a first encryption means for encrypting data outputted from the code ROM;

a second encryption means for generating a read enable signal through an encryption process;

and an output means for dumping out the encrypted data outputted from the first encryption means in response to the read enable signal outputted from the second encryption means." see column 6, lines 13-35; column 6, lines 55-67; column 8, lines 18-25 and figures 3, 4, and 6.

Regarding claim 2, Fleischman meets the claimed limitations as follows: "The apparatus of claim 1, wherein the first encryption means including: a multiple input signature analysis register (MISR) for compressing data outputted from the code ROM in synchronization with a clock signal; and an initializing means for providing an initialization value to the MISR unit in response to a test enable signal and a reset signal." see column 6, lines 13-35; column 6, lines 55-67; column 8, lines 18-25 and figures 3, 4, and 6.

Regarding claim 3, Fleischman meets the claimed limitations as follows: "The apparatus of claim 2, wherein the initializing means includes a transistor, which provides the initialization value to the MISR unit when all the test enable signal and the reset signal are enabled." see column 6, lines 13-35; column 6, lines 55-67; column 8, lines 18-25 and figures 3, 4, and 6.

Regarding claim 4, Fleischman meets the claimed limitations as follows: "The apparatus of claim 1, wherein the second encryption means including: a control state machine unit for generating a control signal for a ROM test operation in response to the test enable signal and the clock signal; a MISR unit for inputting, inputting and

compressing key data in synchronization with the clock signal; an initializing means for providing an initialization value to the MISR unit in response to the test enable signal and the reset signal; and a comparison unit for outputting the read enable signal by comparing a value outputted from the MISR unit with an expected value." see column 6, lines 13-35; column 6, lines 55-67; column 8, lines 18-25 and figures 3, 4, and 6.

Regarding claim 11, Fleischman meets the claimed limitations as follows:

"An apparatus for protecting data outputted from a code ROM, comprising:

a control state machine unit for generating a control signal for a ROM test operation in response to the test enable signal and the clock signal;

a MISR unit for inputting, compressing key data in synchronization with the clock signal in response to the test enable signal;

an initializing means for providing an initialization value to the MISR unit in response to the test enable signal and the reset signal;

a comparison unit for outputting the read enable signal by comparing value outputted from the MISR unit with an expected value; and an output means for dumping the code ROM data in response to a read enable signal." see column 6, lines 13-35; column 6, lines 55-67; column 8, lines 18-25 and figures 3, 4, and 6.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

A. Han (US 5,313,520) discloses a method for protecting data stored in ROM.

B. Caldera (US 5,841,968) discloses a system for testing data from a device.

C. Whetsel (US 2002/0112199) discloses a adaptive system for scan testing a device.

D. Rajski (US 2003/0097614) discloses a method for testing circuits using a Multi-input Signature Register (MISR).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew B. Smithers whose telephone number is (571) 272-3876. The examiner can normally be reached on Monday-Friday (8:00-4:30) EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel L. Moise can be reached on (571) 272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew B Smithers
Primary Examiner
Art Unit 2137